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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,856	02/04/2004	Toshimasa Tanaka		3512

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EXAMINER	
NGUYEN, JIMMY H	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/771,856	TANAKA, TOSHIMASA	
	Examiner	Art Unit	
	Jimmy H. Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *8-17 and 19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 7/15/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is made in response to applicant's RESPONSE TO ELECTION REQUIREMENT AND AMENDMENT, filed on 12/18/2006.

2. Applicant's election without traverse of species I, as illustrated in figures 1-9 in the reply filed on 12/18/2006 is acknowledged.

3. Claims 8-17 and 19 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species II as indicated by the applicant in the RESPONSE TO ELECTION REQUIREMENT, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on 12/18/2006. Claims 1-7 and 18 are considered as follows:

Claim Objections

4. Claim 1 is objected to because of the following informalities:

"unit having:" in line 1 should be changed to -- unit, comprising: --, in order to clarify the claimed invention, i.e., a first voltage conversion circuit, a multiplicity of buffer circuits of the electric power unit, instead of a display unit. See claim 3 as a reference.

"a multiplicity of buffer circuits" in lines 6-7 should be changed to -- a **second** multiplicity of buffer circuits --, in order to make this limitation distinct from the limitation, "a multiplicity of buffer circuits" in line 3.

"(low output voltage group)" in line 8 should be deleted.

"buffers" in line 20 should be changed to -- buffer circuits -- in order to make this limitation consistent with the limitations in lines 3 and in lines 6-7.

Appropriate corrections are required.

5. Claim 18 is objected to because of the following informalities:

"(high output voltage group)" in lines 13-14 should be deleted.

"of side" in line 27 should be deleted.

"first output voltage" in line 32 should be changed to -- said highest output voltage of said high output voltage group --; see Fig. 1.

Appropriate corrections are required.

Notice to Applicant

6. Due to a number of minor informalities presented in the pending claims, Examiner suggests the applicant to review all claims and to make changes as necessary, in order to clarify the claimed invention and to improve their form to conform with U.S. claim drafting practice.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-7 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claims 1-2, independent claim 1 recites the limitation "the order mentioned" in line 6. There is insufficient antecedent basis for this limitation in the claim since it is not clear what the order is mentioned. Further, independent claim 1 recites the limitation, "**said first through third output power supply voltages are provided as the operating voltages of said buffers** ... group" in last 3 lines. Since it is not clear that the above underlined limitation requires all the first through third output power supply voltages provided to one or more buffers, only one of

first through third output power supply voltages provided to one or more of buffers (e.g., the first output power supply voltage provided to the first buffer(s), the second output power supply voltage provided to the second buffer(s), and the third output power supply voltage provided to the third buffer(s)), any combined two of the first through third output power supply voltages provided to one or more buffers, or etc., it is considered that the invention is not clearly defined.

As to claims 3-4, independent claim 3 recites the limitation, "**a multiplicity of buffer circuits for respectively generating output voltages from said first through third output power supply voltages**" in last 2 lines. Since it is not clear that the above underlined limitation requires one or more buffer circuits generating one or more output voltages from all the first through third output power supply voltages, one or more buffer circuits generating one or more output voltages from only one of first through third output power supply voltages (e.g., the first buffer circuit(s) generating one or more output power supply voltages from the first output power supply voltage, the second buffer circuit (s) generating one or more output power supply voltages from the second output power supply voltage, and the third buffer circuit(s) generating one or more output power supply voltages from the third output power supply voltage), one or more buffer circuit(s) generating one or more output power supply voltages from any combined two of the first through third output power supply voltages, or etc., it is considered that the invention is not clearly defined.

As to claims 5-7, independent claim 5 recites the limitation "the order mentioned" in line 8. There is insufficient antecedent basis for this limitation in the claim since it is not clear what the order is mentioned. Further, independent claim 5 recites the limitation, "**all** lower than said first output power supply voltage in the order mentioned" in lines 7-8. Since it is not clear

whether "**all**" includes an inputted power supply voltage presently recited in lines 2-3, it is considered that the invention is not clearly defined.

As to claim 18, this claim recites the limitation "the order mentioned" in line 18. There is insufficient antecedent basis for this limitation in the claim since it is not clear what the order is mentioned. Further, independent claim 5 recites the limitation, "**all** lower than said first output power supply voltage in the order mentioned" in lines 7-8. Since it is not clear whether "**all**" includes an inputted power supply voltage presently recited in lines 2-3, it is considered that the invention is not clearly defined.

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claims 1-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As to claims 1-2, independent claim 1 contains the limitation, "**said first through third output power supply voltages are provided as the operating voltages of said buffers ... group**" in last 3 lines. As discussed in the above rejection under 35 USC 112, second paragraph, Examiner assumes that the above underlined limitation requires all the first through third output power supply voltages provided to one or more buffers, only one of first through third output power supply voltages provided to one or more of buffers (e.g., the first output power supply voltage provided to the first buffer(s), the second output power supply voltage provided to the

second buffer(s), and the third output power supply voltage provided to the third buffer(s)), or any combined two of the first through third output power supply voltages provided to one or more buffers. However, the original disclosure, specifically Fig. 1 and the corresponding description, expressly teaches a first buffer (B0) provided with a first output power supply voltage (Vout1) and a ground voltage (Vgnd), two first buffers (B1, B2) provided with a first output power supply voltage (Vout1) or an output voltage (V0) of the first buffer and a second output power supply voltage (Vout2), and two first buffers (B3, B4) provided with a third output power supply voltage (Vout3) and a ground voltage (Vgnd). Accordingly, these claims contain the above underlined limitation, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As to claims 3-4, independent claim 3 contains the limitation, "**a multiplicity of buffer circuits for respectively generating output voltages from said first through third output power supply voltages**" in last 2 lines, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. See the above rejection under 35 U.S.C. 112, first paragraph, to claims 1-2.

As to claims 5-7, independent claim 5 contains the limitation, "**a reference voltage generating circuit that generates ... a six voltage based on said first output power supply voltage**" presently recited in lines 4-7. As best understood in light of the disclosure, specifically Fig. 1 and the corresponding description, Applicant means the claimed reference voltage generating circuit, which comprises elements (A1, R1-R4) and connections as shown in Fig. 1,

and the claimed six voltage corresponding to the ground voltage (Vgnd). However, Examiner notes that there is nowhere in the specification to disclose the ground voltage (i.e., the claimed six voltage) generated based on the first output power supply (Vout1), as presently claimed. Further, a person of ordinary skilled in the art would know that the input power supply voltage (Vcc) and the ground voltage must be supplied together since the voltage level (e.g., Vcc = 3V, see page 12, lines 5-6) is measured with respect to the ground voltage. Accordingly, these claims contain the above underlined limitation, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tsuchiya (US 7,061,481 B2) discloses a related display device (see Fig. 1) comprising an electric power unit (10), which comprises a first step-up circuit (12); a regulator (14) for stabilizing the output voltage (Vout) of the first step-up circuit (12) and stepping down to a voltage (Vc); a second step-up circuit (16); and a multipotential generating circuit (18) for generating a plurality of output voltages. See Figs. 3-8 and the corresponding description.

Nanno et al. (US 6,909,413 B2) discloses a related display device (see Fig. 2) comprising an electric power unit (24), which comprises a first step-up circuit (CP1); a second step-up circuit (CP2); and a third step-up circuit (CP3), for generating output voltages used to drive the display unit. See Figs. 4-5 and the corresponding description.

Yanagi et al. (US 7,126,595 B2; see Figs. 10, 12, 15 and 16), Ito (US 6,426,594 B1; see Figs. 14, 16 and 17); and Tanaka (US 6,326,959 B1; see Figs. 1-3) all discloses a related display device comprising an electric power unit having one or more step-up circuits and/or one or more step-down circuits, for generating output voltages used to drive the display unit.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is 571-272-7675. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JHN
January 31, 2007

Jimmy H. Nguyen
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